FASTBUS BACKPLANE IMPEDANCE

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In order to specify the backplane impedance some assumptions must be made:

1. An attempt will be made to keep the impedance as high as possible using ordinary manufacturing tolerances for the laminates and P. C. boards.

2. The pins currently used will continue to be used in the future.

In discussions with several manufacturers of metal clad laminates and P. C. boards, the following tolerances were acquired:

A. Laminate:

1. | Copper thickness | Nominal thickness | Range |
    | --- | --- | --- |
    | 1 oz. | 1.4 mils. | 1.2 to 1.6 mils. |
    | 2 oz. | 2.8 mils. | 2.5 to 3.1 mils. |
    | 3 oz. | 4.2 mils. | 3.8 to 4.6 mils. |

2. Dielectric thickness: G-10, FR-4, or FR-5

    For thickness greater than .020", the tolerance is about ±10% over 90% of the area, but should not exceed ±12.5% of the specified thickness anywhere.

3. Dielectric constant: should not exceed 5.4

    The range is about 4.3 - 5.4
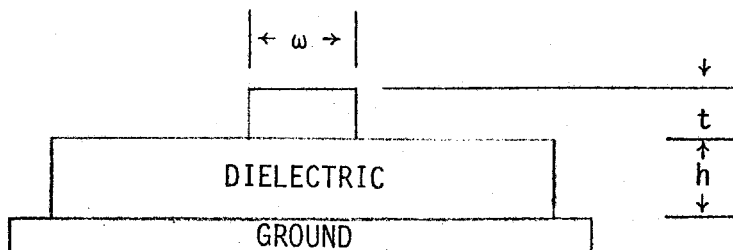
B. P. C. Boards:

1. Plating variation: ±25% of nominal thickness

2. Etching: line width variation is ±2X times laminate copper thickness

From the Motorola and Fairchild ECL design handbooks, the characteristic impedance for microstrip lines is given as:

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \ell n \left(\frac{5.98\ h}{.8\omega + t} \right)$$

where

and

E_r = the dielectric constant

In order to gain a large Z_0 we would like small E_r, ω, and t and large h.

If we select standard P. C. board material, the range of E_r is 4.3 - 5.4 (much lower and more controlled dielectric constant materials are available, if necessary).

A minimum line width of about .007 should be selected to minimize production waste.

The finished line thickness should be .0024", although the lower, the better.

The range of characteristic impedance one might expect, using 1 oz. copper on .060" board plated up 0.7 oz. (.75 to 1.25 mils.), would be determined as follows:

ω	h	t	E_r	Z_0
.0102	.054	.00285	5.4	112.64 min.
.007	.060	.0024	4.85	132.25 nom.
.0046	.066	.00195	4.3	154.73 max.

The propagation delay for these lines is on the order of 150 pico second per inch which gives a distributed capacity of:

$$C_0 = \frac{150 \times 10^{-12}}{Z_0}$$

or

Z_0	C_0
113	1.33 pF/inch
132	1.14 pF/inch
155	0.97 pF/inch

The impact of the pins in the back plane on impedance can be determined:

$$Z_0 \text{ pins} = \frac{Z_0 \text{ no pins}}{\sqrt{1 + \dfrac{C_D}{C_0}}}$$

The pins produce 2.05 pF/pin or 3.15pF/inch

Z_0 NO PINS	Z_0 PINS
113	61.6Ω
132	68.
155	75.

Thus one can see that taking the standard run of the mill P. C. boards one might expect an impedance in the range of 60 to 75Ω.

Once modules are plugged into the slots with the associated capacitance of at least 10pF per slot or:

$$\frac{10pF}{SLOT} \cdot \frac{SLOT}{0.65 \text{ INCH}} = \frac{15.4pF}{INCH}$$

the line impedance becomes approximately:

Z_0 pins	Z_0 modules
61.6Ω	29.2Ω
68.	31.8
75.	34.6

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